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(54) Abstract Title
Electronic module interconnection including a switch array to simulate fault conditions

(57) A test arrangement for simulating fault conditions in a multiple-channel cable comprising an array of switches which includes switches which are connected in series with respective channels of the cable. The arrangement may include a socket S3 and a plug P3, each provided with a pair of RS 232 line driver / receiver modules IC1 - 4, on either end of the cable. The switches may be a cross-bar switch array IC8 connected to a microprocessor PC which controls the RS 232 modules so as to simulate a sequence of interconnection failures within the cable. The failures can be applied and removed in rapid succession to the electronic modules on either end of the arrangement with reduced risk of damage to the electronic modules. The arrangement may be used to test the operation of built-in test means on the electronic modules.

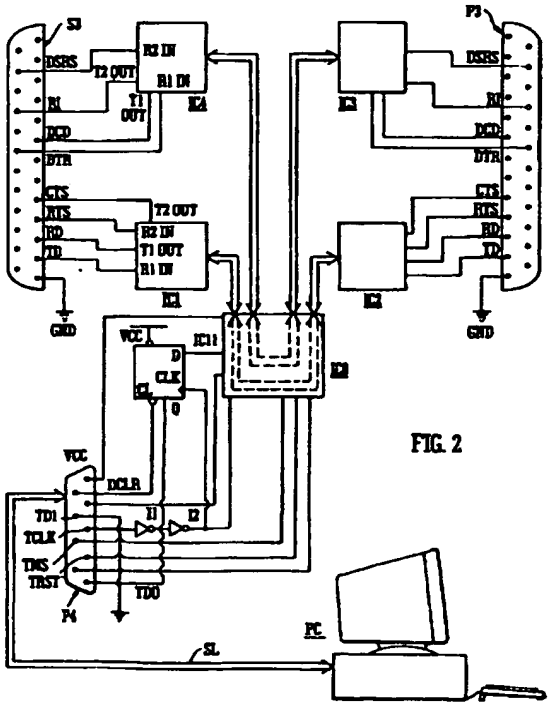

FIG. 2

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

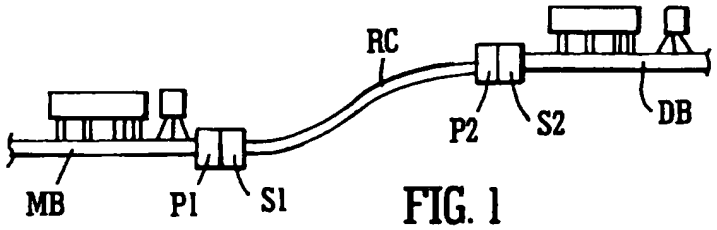

RC
P2
S2
DB
MB
P1
S1

FIG. 1

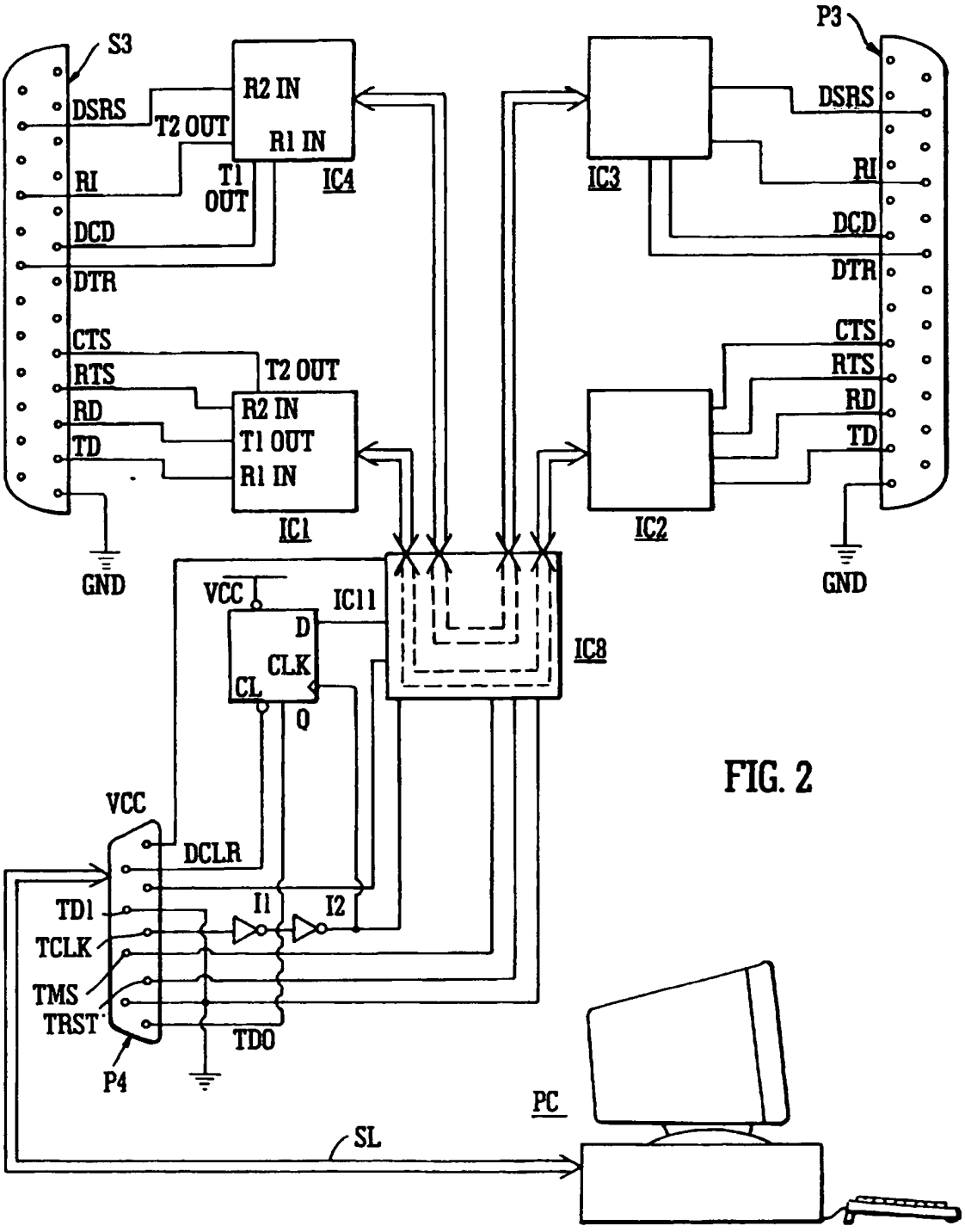

S3
DSRS
T2 OUT
R2 IN
R1 IN
RI
T1 OUT
IC4
DCD
DTR
CTS
RTS
T2 OUT
RD
R2 IN
TD
T1 OUT
R1 IN
IC1
GND
IC3
P3
DSRS
RI
DCD
DTR
CTS
RTS
RD
TD
IC2
GND
VCC
IC11
D
CLK
CL
Q
IC8
VCC
DCLR
TDI
TCLK
TMS
TRST
I1
I2
TDO
P4
PC
SL

FIG. 2

FIG. 3

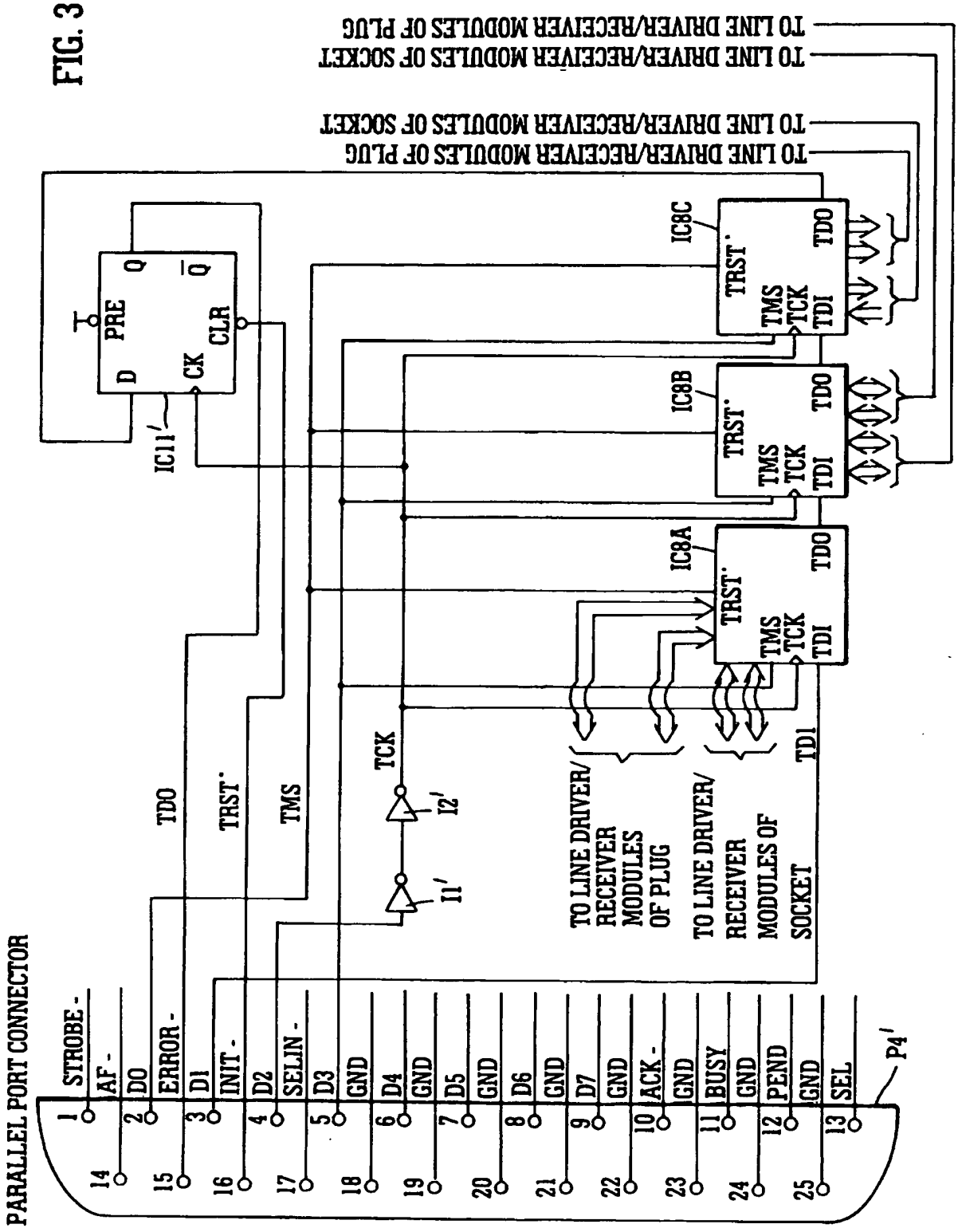
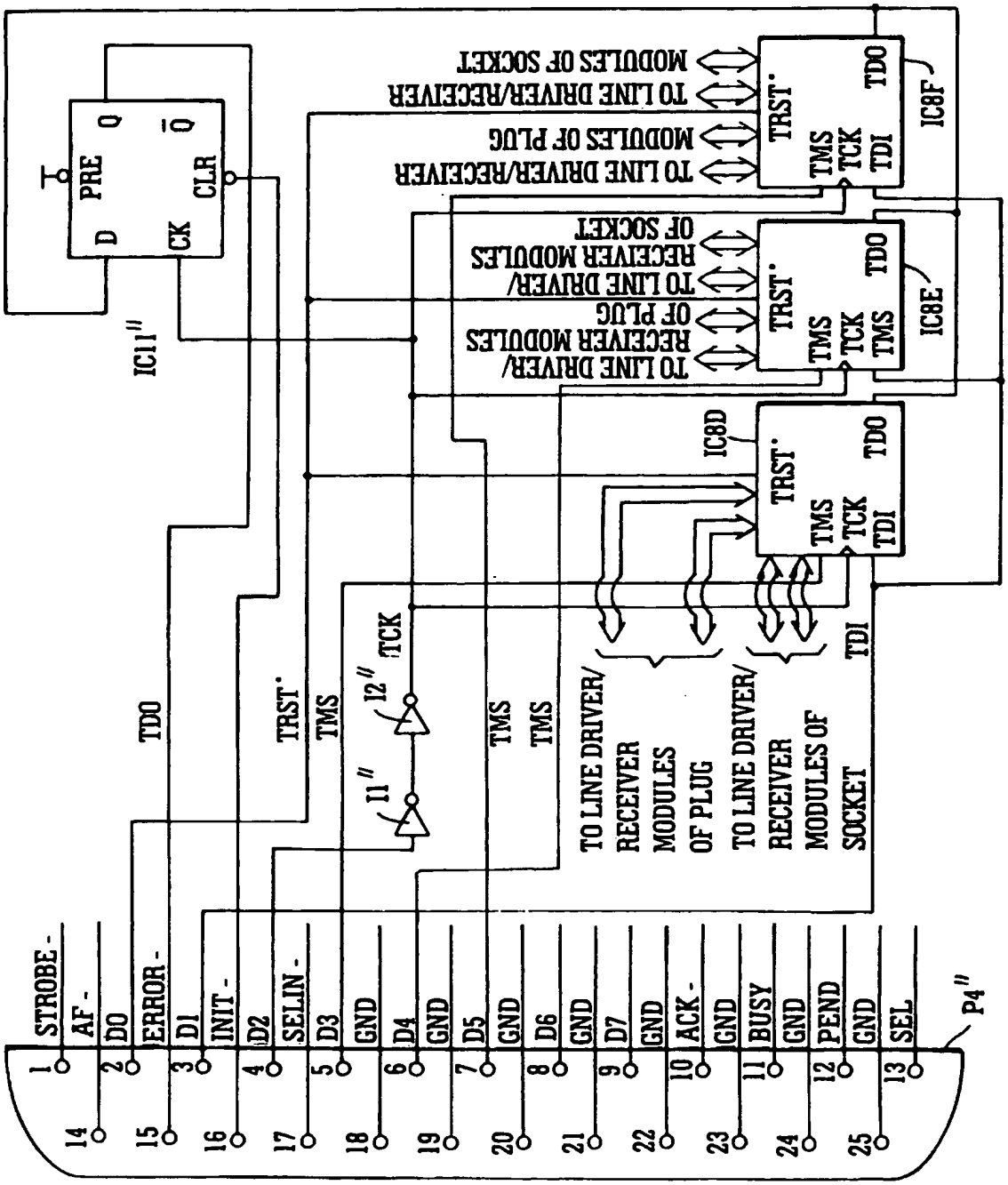

PARALLEL PORT CONNECTOR
STROBE-
AF-
DO
ERROR-
D1
INIT-
D2
SELIN-
D3
GND
D4
GND
D5
GND
D6
GND
D7
GND
ACK-
GND
BUSY
GND
PEND
GND
SEL
P4'
TDO
TRST'
TMS
TCK
I1'
I2'
IC11'
D
CK
PRE
CLR
Q
IC8A
IC8B
IC8C
TRST'
TMS
TCK
TDI
TDO
TD1
TO LINE DRIVER/ RECEIVER MODULES OF PLUG
TO LINE DRIVER/ RECEIVER MODULES OF SOCKET
TO LINE DRIVER/RECEIVER MODULES OF SOCKET
TO LINE DRIVER/RECEIVER MODULES OF PLUG

FIG. 4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AF-
D0
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D1
INIT-
D2
SELIN-
D3
GND
D4
GND
D5
GND
D6
GND
D7
GND
ACK-
GND
BUSY
GND
PEND
GND
SEL
TDO
TRST'
TMS
TCK
TDI
I1''
I2''
IC11''
IC8D
IC8E
IC8F
TO LINE DRIVER/ RECEIVER MODULES OF PLUG
TO LINE DRIVER/ RECEIVER MODULES OF SOCKET
MODULES OF SOCKET
TO LINE DRIVER/RECEIVER
MODULES OF PLUG
TO LINE DRIVER/RECEIVER
TO LINE DRIVER/ RECEIVER MODULES OF SOCKET
TO LINE DRIVER/ RECEIVER MODULES OF PLUG
TO LINE DRIVER/ RECEIVER MODULES OF SOCKET
PRE
CLR
CK
D
Q
Q̄

TESTING ARRANGEMENT

The present invention relates to a testing arrangement for simulating a failure in a multi-channel signal or power link.

Most modern items of electronic equipment of significant complexity are of modular construction and have suitable signal links (e.g. in the form of ribbon cables and associated removable connectors) connecting the different modules. Therefore the present invention is particularly applicable to the testing of such modular electronic equipment.

Failure effect mitigation is a factor of equipment design which is becoming increasingly important to purchasers of complex electronic systems. Unless failure modes are considered in detail during the design phase, the equipment is unlikely to meet the purchaser's specification with regard to reliability and maintainability. Such design shortcomings will adversely affect through life up-keep and repair costs and may easily result in rejection of the final equipment. In many cases also, the failure modes have profound effects on safety. Electronic equipment presents a particularly difficult problem with ever more and more functionality being reduced to minute physical spaces and much of it dependent on correctly functioning software to work at all.

One failure mitigation concept, that of Built In Test (BIT), has been refined to the point where it is routinely included in equipment specifications with the added requirement to quantify its effectiveness. It has always been a difficult task because the ground work must b laid during the early stages of

development but the effectiveness may not be proven (or otherwise) until many years later. During the intervening period, the equipment supplier and purchaser are at risk of an unsatisfactory outcome to a reliability or maintainability demonstration. At worst it may result in rejection and at best it may result in acrimony because it is just too difficult to prove one way or another. The equipment development phase will most likely be over and hence the rectification costs must be borne during the most costly phase of the project.

Temporary failure insertion is a means of testing the effectiveness of BIT and the accuracy of failure isolation time predictions for maintainability. It is a concept that has been around for a long time in its simplest form but it has become increasingly difficult to perform cost effectively with the growth of equipment complexity.

In particular, there is a risk of damage to the equipment if a failure is inserted, (e.g. by breaking a connection or causing a short-circuit) and certain types of failure such as conditional failures are difficult or impossible to simulate by conventional methods.

An objective of the present invention is to overcome or alleviate the above difficulties.

In one aspect the invention provides a testing arrangement for simulating a failure in a multi-channel signal or power link, the testing arrangement comprising an electronically controlled switching array connected in series in the link and arranged to control signal transmission through the channels

individually, the switching array having a fault-simulating state in which normal signal transmission is disrupted.

Preferably the switching array has a plurality of input terminals and a corresponding plurality of output terminals and processing means connected between the input and output terminals and arranged in one state to generate an output signal at an output terminal corresponding to an input signal detected at a corresponding input terminal, thereby allowing normal signal transmission through the link, the processing means being arranged in the fault-simulating state to generate at an output terminal an output signal which does not correspond to the input signal at the corresponding input terminal, thereby simulating a fault.

In a preferred embodiment the switching array is controlled by a programmed microprocessor, the program defining a sequence of switching states of the array representing different fault conditions.

This feature leads to the advantages that a complex sequence of fault conditions can be applied and removed very rapidly, minimising the risk of irreversible damage to the equipment and also enabling a variety of complex fault conditions to be simulated in a repeatable manner.

Preferably the switching array is provided with a local memory arranged to store program data prior to execution by said microprocessor. This feature enhances the flexibility of the arrangement.

Preferably the switching array has a control interface coupled to a personal computer, the computer being arranged to select, under program control, a sequence of fault states stored in said local memory. This feature provides further flexibility and enables remote testing.

Preferably the switching array is arranged to apply and then remove the fault-simulating state in a period of less than 5 milliseconds, more preferably less than one millisecond, desirably less than 100 nanoseconds.

Further preferred features of the invention are defined in the dependent claims.

A preferred embodiment is described below by way of example only with reference to Figures 1 to 4 of the accompanying drawings, wherein:

Figure 1 is a somewhat schematic side elevation of modular electronic equipment suitable for testing with the arrangement of the present invention;

Figure 2 is an electronic block diagram of a testing arrangement of the invention;

Figure 3 is a block diagram of a second embodiment, and

Figure 4 is a block diagram of a third embodiment.

Referring to Figure 1, a motherboard MB populated with electronic components has a 25-pin plug P1 removably connected to a complementary socket S1 of a

ribbon cable RC, having a 25-pin plug P2 at its other end similarly connected to a socket S2 of a daughter board DB which is also populated with electronic components. Signals (e.g. RS 232 signals) as well as earth and power connections are carried by the ribbon cable RC between the two boards MB and DB.

In order to test the above equipment, the arrangement of Figure 2 is provided and is substituted for the ribbon cable RC and its associated socket S1 and plug P2 in the equipment of Figure 1 by plugging plug P1 into a socket S3 of the testing arrangement and by plugging a plug P3 of the testing arrangement into socket S2 of the equipment.

The testing arrangement comprises a pair of line driver/line receiver modules IC1 and IC4 each having their communication terminals R1 IN, R2 IN, TI OUT and T2 OUT connected to corresponding pins of socket S3 and a similar pair of line driver/line receiver modules IC2 and IC3 having their communication terminals connected to corresponding pins of plug P3. Each of the above modules has two RS 232 inputs R1 IN and R2 IN and two RS 232 outputs T1 OUT and T2 OUT.

The above pairs of modules are controlled at TTL or CMOS control inputs thereof by a PS48 cross bar switch device IC8 so as effectively form a back-to-back connection as indicated by the dashed buses shown in IC8. In the transparent state, IC8 detects, via IC1 and IC4, signals at the DSRS (Data Signalling Rate Select), RI (Ring Indicator), DCD (Data Carrier Detect), DTR (Data Terminal Reading), CTS (Clear to Send), RTS (Revert to Send), RD (Receive Data) and TD (Transmit Data), pins of socket S3 and generates, via IC2 and IC3,

corresponding signals at the corresponding pins of plug P3, or vice-versa. A variety of other states can be set by IC8, all of which simulate faults.

The ports of the PS48 device, IC8, may be programmed as inputs or outputs via its test access port. A JTAG (Joint Test Action Group) interface comprising a plug P4 loads a serial data stream into the PS48 device on the Test Data In (TDI) line to set up the device and at the same time down loads data from the PS48 device via the Test Data Out (TDO) line. TDO might be results from a previous test.

Data is clocked into and out of the PS48 device on the rising edge of a TTL level clock signal TCLK provided with the data from a personal computer PC via a serial link SL.

Because several failure insertion devices may be used together and controlled from a single PC, there is a Test Mode Select (TMS) line which has to be active in order that the PS48 device responds correctly.

A Test Mode ReSet (TMRS) line is provided to reset the device to an unconfigured state.

The device IC8 is provided with a D-type flip flop device IC11 which receives clock signals from the computer PC via inverters I1 and I2 and has its incoming data stream clocked by the rising edge of the Test Clock (TCLK) signal. In the Test Mode, the state of the output pins is serially clocked on the falling edge of TCLK.

The device IC8 incorporates static RAM (not shown) which stores a set of switching states representing different failure modes and these can be downloaded from the computer PC. These locally stored states are selected and applied in a user-selected programmed service by the computer PC which is suitably programmed. The failures may be static, dynamic, sequential, conditional, intermittent or combinational.

Four modes of operation of the device IC8 can be selected with attributes as shown in Table 1 below:

TABLE 1

i) Pins programmed as logic outputs from the subject assembly

No failure	Open circuit/ tristated	Stuck at logic HIGH	Stuck at logic LOW

1 output connected to N outputs (1-N isolated from source)

ii) Pins programmed as analogue outputs from the subject assembly

No failure	Open circuit	1 output connected to N outputs (1-N isolated from source)

iii) Pins programmed as logic inputs to the subject assembly

No failure	Open circuit/ tristated	Stuck at Logic HIGH (isolated from source)

Stuck at Logic LOW (isolated from source) Input connected to N inputs (1-N isolated from source)

iv) Pins programmed as power or high fanout outputs

No failure	Open circuit	Short circuit (current limited)

v) Pins programmed as power inputs

No failure	Open circuit	Short circuit (current limited)

The arrangement shown in Figure 3 comprises three PS48 cross-bar switch devices IC8A, IC8B and IC8C similar to device IC8 of Figure 2 and each having two data buses connected to respective line driver/receiver modules (not shown, but similar to modules IC2 and IC3 of Figure 2) of a plug and two data buses connected to respective line driver/receiver modules (not shown, but similar to modules IC1 and IC4 of Figure 2) of a socket. The above plug (not shown) may be a common plug similar to plug P3 of Figure 2 but with three sets of the relevant pins connected to the respective three pairs of line driver/receiver modules or each of switch devices IC8A, IC8B and IC8C may be connected via its associated line driver/receiver modules to an individual plug identical to plug P3 of Figure 2. Similarly the above socket (not shown) may be a common socket similar to socket S3 of Figure 2 but with three sets of the relevant pins connected to the three respective pairs of line driver/receiver modules or one or more of switch devices IC8A, IC8B and IC8C may be connected via its associated line driver/receiver modules to an individual socket identical to socket S3 of Figure 2. The plug arrangement will normally correspond to the socket arrangement (i.e. one plug + one socket or three plugs + three sockets) but need not do so, depending on the nature of the circuitry under test.

The TDI (Test Data In)/TDO (Test Data Out) pairs of IC8A to IC8C are connected in series between TDI input pin 3 of a JTAG plug P4' (similar to plug P4 of Figure 2) and an input pin of a D-type flip-flop device IC 11' (similar to IC 11 of Figure 2) whose corresponding ouput pin is connected to the TDO (Test Data Out) output pin of plug P4'.

The switching devices IC8A to IC8C are clocked in synchronism with a common clock signal TCK from the series-connected inverter combination I1' and I2' and

are simultaneously put in test mode by means of a common TMS (Test Mode Select) signal from plug P4' going HIGH. In this state the switching devices are connected in series at their TDI and TDO ports. Each switching device is then programmed conventionally by a serial data stream from a personal computer (not shown) via the TDI line from plug P4'. When the personal computer has determined (by counting clock pulses) that IC8A and IC8B and IC8C are full, it sets the TMS line LOW to run the resulting stored switching program in IC8A, IC8B and IC8C simultaneously.

The above arrangement is suitable for testing circuitry in which faults in one circuit link (e.g. a link in which the line driver/receiver modules (not shown) of IC8A are inserted) affect the behaviour of another circuit link (e.g. a link in which the line driver/receiver modules, not shown, of IC8B are inserted).

The test program loaded into IC8A may optionally be different from that loaded into IC8B and the test program loaded into IC8C may optionally be different from that loaded into IC8B.

Figure 4 shows an arrangement similar to that of Figure 3 except that each PS48 cross-bar switch IC8D, IC8E and IC8F is individually put in test mode (alone or in any desired order) with a different TMS (Test Mode Select) line, and the TDI (Test Data In) inputs are paralleled, as are the TDO outputs. The serial data stream necessary to program the selected PS48 cross-bar switch is then sent from a personal computer (not shown) connected to plug P4' via the TDI line common to the three PS48 cross-bar switches and returned via their respective TDI lines. Although all the PS48 switches are loaded with the switching program, only the selected PS48 switch(es) run the program, under

control of the TMS line. Typically, only one device IC8D, IC8E or IC8F is active at any given time. Hence the circuit links associated with any of these devices (via the associated pairs of line driver/receiver modules, not shown, which are however similar to pairs IC1 + IC4 or IC2 + IC3 of Figure 2) are tested independently.

Whichever cross-bar switching device is selected is clocked by clock signal TCK from the series – connected inverter combination I1" and I2".

There is no practical limit to the number of cross-bar switching devices which can be connected in such a configuration – for example, up to seven such devices can be controlled via a parallel port connector P4".

The arrangement of Figure 3 is suitable for running three different test switching programs in switching devices IC8A, IC8B and IC8C respectively whereas the arrangement of Figure 4 is suitable for running a common switching program in each of devices IC8D, IC8E and IC8F.

CLAIMS

1. A testing arrangement for simulating a failure in a multi-channel signal or power link, the testing arrangement comprising an electronically controlled switching array connected in series in the link and arranged to control signal transmission through the channels individually, the switching array having a fault-simulating state in which normal signal transmission is disrupted.

2. A testing arrangement as claimed in Claim 1, wherein the switching array has a plurality of input terminals and a corresponding plurality of output terminals and processing means connected between the input and output terminals, the processing means being arranged in one state to generate an output signal at an output terminal corresponding to an input signal detected at a corresponding input terminal, thereby allowing normal signal transmission through the link, the processing means being arranged in the fault-simulating state to generate at an output terminal an output signal which does not correspond to the input signal at the corresponding input terminal, thereby simulating a fault.

3. A testing arrangement as claimed in Claim 1 or Claim 2, wherein the switching array is controlled by a programmed microprocessor, the program defining a sequence of switching states of the array representing different fault conditions.

4. A testing arrangement as claimed in Claim 3, wherein the switching array is provided with a local memory arranged to store program data prior to execution by said microprocessor.

5. A testing arrangement as claimed in Claim 4, wherein the switching array has a control interface coupled to a personal computer, the computer being arranged to select, under program control, a sequence of fault states stored in said local memory.

6. A testing arrangement as claimed in any preceding claim, wherein the switching array is arranged to apply and then remove the fault-simulating state in a period of less than 5 milliseconds.

7. A testing arrangement as claimed in Claim 6, wherein said period is less than one millisecond.

8. A testing arrangement as claimed in Claim 7, wherein said period is less than 100 nanoseconds.

9. A testing arrangement as claimed in any preceding claim, wherein an input bus of the switching array is coupled to an output bus of a line receiver whose input bus is coupled to an input end of the multi-channel signal link and an output bus of the switching array is coupled to an input bus of a line driver whose output bus is coupled to an output end of the multi-channel signal link, the switching array being responsive to one or more outputs of the line receiver to generate a signal at one or more inputs of the line driver.

10. A testing arrangement as claimed in claim 9, wherein the switching array has a transparent state in which an input signal received in a given channel from the input end of the multi-channel signal link is reproduced in that channel at the output end of the multi-channel signal link.

11. A testing arrangement as claimed in Claim 9 or Claim 10, which comprises a line driver and receiver coupled to one end of the multi-channel signal link and a further line driver and receiver connected to the other end of the multi-channel signal link, both line drivers and both line receivers being controllable by the switching array whereby faults in bi-directional transmission can be simulated.

12. A testing arrangement as claimed in any preceding claim, comprising two or more programmable switching arrays arranged to be programmed sequentially via a common data input line.

13. A testing arrangement as claimed in any preceding claim, comprising two or more programmable switching arrays arranged to be programmed in parallel via a common data input line.

14. A testing arrangement substantially as described hereinabove with reference to Figure 2 or Figure 3 or Figure 4 of the accompanying drawing.

Amendments to the claims have been filed as follows

1. A testing arrangement for simulating a failure in a multi-channel signal or power link, the testing arrangement comprising an electronically controlled switching array connected in series in the link and arranged to control signal transmission through the channels individually, the switching array having a plurality of input terminals and a corresponding plurality of output terminals and processing means connected between the input and output terminals, the processing means being arranged in one state to generate an output signal at an output terminal corresponding to an input signal detected at a corresponding input terminal, thereby allowing normal signal transmission through the link, the processing means being arranged in the fault-simulating state to generate at an output terminal an output signal which does not correspond to the input signal at the corresponding input terminal, thereby simulating a fault.

2. A testing arrangement as claimed in Claim 1, wherein the switching array is controlled by a programmed microprocessor, the program defining a sequence of switching states of the array representing different fault conditions.

3. A testing arrangement as claimed in Claim 2, wherein the switching array is provided with a local memory arranged to store program data prior to execution by said microprocessor.

4. A testing arrangement as claimed in Claim 3, wherein the switching array has a control interface coupled to a personal computer, the computer being arranged to select, under program control, a sequence of fault states stored in said local memory.

5. A testing arrangement as claimed in any preceding claim, wherein the switching array is arranged to apply and then remove the fault-simulating state in a period of less than 5 milliseconds.

6. A testing arrangement as claimed in Claim 5, wherein said period is less than one millisecond.

7. A testing arrangement as claimed in Claim 6, wherein said period is less than 100 nanoseconds.

8. A testing arrangement as claimed in any preceding claim, wherein an input bus of the switching array is coupled to an output bus of a line receiver whose input bus is coupled to an input end of the multi-channel signal link and an output bus of the switching array is coupled to an input bus of a line driver whose output bus is coupled to an output end of the multi-channel signal link, the switching array being responsive to one or more outputs of the line receiver to generate a signal at one or more inputs of the line driver.

9. A testing arrangement as claimed in Claim 8, wherein the switching array has a transparent state in which an input signal received in a given

channel from the input end of the multi-channel signal link is reproduced in that channel at the output end of the multi-channel signal link.

10. A testing arrangement as claimed in Claim 8 or Claim 9, which comprises a line driver and receiver coupled to one end of the multi-channel signal link and a further line driver and receiver connected to the other end of the multi-channel signal link, both line drivers and both line receivers being controllable by the switching array whereby faults in bi-directional transmission can be simulated.

11. A testing arrangement as claimed in any preceding claim, comprising two or more programmable switching arrays arranged to be programmed sequentially via a common data input line.

12. A testing arrangement as claimed in any preceding claim, comprising two or more programmable switching arrays arranged to be programmed in parallel via a common data input line.

13. A testing arrangement substantially as described hereinabove with reference to Table 1.

14. A testing arrangement substantially as described hereinabove with reference to Figure 2 or Figure 3 or Figure 4 of the accompanying drawing.

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Applicati n No:	GB 9820289.8	**Examiner:**	John Watt
Claims searched:	1 - 14	**Date of search:**	2 February 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): G1U (UR3100, UR3128, UR31317)

Int Cl (Ed.7): G01R 31/00, 31/28, 31/3187, 31/319

Other: Online: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0585769 A1	(FIAT AUTO) see figs.1 - 3 and col.1, line 28 to col.2, line 8	1 - 5 at least
X	US 5798647	(CHRYSLER) see figs.1 - 3 and col.2, lines 24 - 41	1 at least
X	US 5739694	(LIVERNOIS RESEARCH) see whole document	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.